IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) An event pipeline and summing apparatus for processing event data stored in an event memory of an event based test system, comprising:

an event count delay logic which produces a gross delay of event count data, which is an integral part of the event data, by counting a clock ~~for~~ by a number of ~~time~~ times defined by the event count data;

a vernier data decompression logic which reproduces event vernier data which is a fractional part of the event data;

an event vernier summing logic which produces event vernier sum data by summing the vernier data from the vernier data decompression logic; and

an event scaling logic which changes the event count data from the event count delay logic and the event vernier data from the event vernier summing logic in proportion to a scale factor;

wherein ~~one or more~~ a plurality of parallel pipelines are incorporated at least in the event vernier summing logic for processing the event vernier data in parallel where each pipeline is configured by a plurality of series connected registers.

2. (Currently Amended) An event pipeline and summing apparatus as defined in Claim 1, further comprising a window strobe

logic which ~~causes~~ operates to generate a window strobe when event data of two consecutive events match with one another.

3. (Currently Amended) An event pipeline and summing apparatus as defined in Claim 1, wherein said event count data for each event is configured by one or more words where each word of said event count data is stored in a different address of the event memory.

4. (Original) An event pipeline and summing apparatus as defined in Claim 1, wherein said event vernier data for each event is configured by vernier delay data and event type data, and wherein said event vernier data for each event is divided into one or more segments, and wherein each segment of said event vernier data is stored in the same or different address of the event memory.

5. (Currently Amended) An event pipeline and ~~summating~~ summing apparatus as defined in Claim 1, wherein the event count delay logic includes;

an event counter which loads the event count data and counts the event count data by the clock and produces a terminal count signal when a count result reaches a predetermined value; and

a state machine which controls an overall operation of the event pipeline and summing ~~logic~~ apparatus including a process for loading the event count data into the event counter and a process for generating an event trigger signal

in response to the terminal count signal from ~~he~~ the event counter.

6. (Currently Amended) An event pipeline and summing apparatus as defined in Claim 1, wherein said event vernier data for each event is divided into one or more segments, and wherein said vernier data decompression logic includes:

a plurality of pre-fetch registers to pre-fetch the one or more segments of the event vernier data;

a plurality of loop storage registers which store the vernier data from the pre-fetch registers for performing a loop operation on the segments of the event vernier data; and

a state machine which controls an operation of the vernier data decompression logic including at least an operation of the pre-fetch registers and loop storage registers.

7. (Original) An event pipeline and summing apparatus as defined in Claim 1, wherein said event vernier data for each event is divided into base vernier and one or more other verniers, and wherein said event vernier summing logic includes:

a base accumulator which accumulates vernier delays of the base verniers for all of previous and current events;

a plurality of accumulators which accumulate vernier delays of other verniers for all of previous and current events on an accumulated result of the base verniers from the base accumulator; and

a state machine which controls an overall operation of the event vernier summing logic including sending an instruction to the event scaling logic to insert one cycle of wait state into a current event count cycle when a carry arises in accumulating the vernier delays.

8. (Original) An event pipeline and summing apparatus as defined in Claim 1, wherein the event scaling logic includes:

an event vernier scaling logic which produces an event enable signal for each pipeline by scaling the vernier sum data from the event vernier summing logic by the scale factor; and

an event count scaling logic which produces an event clock based on the scale factor and provides the event clock to the event count delay logic.

9. (Original) An event pipeline and summing apparatus as defined in Claim 8, wherein said event count scaling logic includes:

a scaling counter logic for counting the clock when the event count scaling starts;

a comparator which compares an output of the scaling counter logic and the scale factor and produces a terminal count signal when the output of the scaling counter logic reaches a value one less than the scale factor; and

an AND logic which produces the event clock based on the terminal count signal from the comparator and an extra cycle request from the event vernier summing logic.

10. (Original) An event pipeline and summing apparatus as defined in Claim 8, wherein said event vernier scaling logic includes:

an accumulator for accumulating the vernier sum data from the event vernier summing logic by a number of times one less than the scale factor.

11. (Currently Amended) An event pipeline and summing apparatus as defined in Claim 2, wherein the window strobe logic includes:

a vernier data comparison logic which differentiates a window strobe event from other events by comparing event type data of two consecutive events and provides a window strobe signal to the event ~~vernier~~ scaling logic.

12. (Currently Amended) An event pipeline and summing method for processing event data stored in an event memory of an event based test system, comprising the following steps of:

producing a gross delay of event count data, which is an integral part of the event data from ~~an~~ the event memory, by counting a clock ~~for~~ by a number of ~~time~~ times defined by the event count data;

decompressing event vernier data which is a fractional part of the event data ~~compressed~~ in the event memory;

summing the event vernier data based on the decompressed event vernier data through a plurality of pipelines arranged in parallel and ~~**shifts**~~ shifting the event vernier data at each timing of the clock to produce event vernier sum data where each pipeline is configured by a plurality of series connected registers; and

modifying the event count data and the event vernier data in proportion to a scale factor.

13. (Currently Amended) An event pipeline and summing method as defined in Claim 12, further comprising the step of interpreting the event vernier data and generating a window strobe when the event vernier data of two consecutive events match with one another.

14. (Original) An event pipeline and summing method as defined in Claim 12, wherein said step of producing the gross delay of event count data includes the steps of:

counting the event count data by the clock and producing a terminal count signal when a count result reaches a predetermined value; and

generating an event trigger signal in response to the terminal count signal.

15. (Original) An event pipeline and summing method as defined in Claim 12, wherein said event vernier data for each event is divided into base vernier and one or more other verniers, and

wherein said step of summing the event vernier data includes the steps of:

accumulating vernier delays of the base verniers for all of previous and current events;

accumulating vernier delays of other verniers for all of previous and current events on an accumulated result of the base verniers; and

requesting an insertion of one cycle of wait state into a current event count cycle when a carry arises in accumulating the vernier delays.

16. (Original) An event pipeline and summing method as defined in Claim 12, wherein said step of modifying the event count data and the event vernier data includes the steps of:

scaling the vernier sum data by the scale factor and producing an event enable signal for each pipeline; and

producing an event clock based on the scale factor and producing the gross delay of event count data by counting the event clock.

17. (Currently Amended) An event pipeline and summing method as defined in Claim 16, wherein said step of producing the event clock includes the steps of:

counting the clock;

comparing the count result ~~and the scaling counter logic~~ and the scale factor and producing a terminal count signal

when the count result reaches a value which is one less than the scale factor; and

generating the event clock based on the terminal count signal.

18. (Original) An event pipeline and summing method as defined in Claim 17, wherein said step of scaling the vernier sum data by the scale factor includes a step of accumulating the vernier sum data by a number of times one less than the scale factor.

19. (Currently Amended) An event pipeline and summing method as defined in Claim ~~12~~ 13, wherein said step of generating the window strobe ~~logic~~ includes a step of differentiating a window strobe event from other events by comparing event type data of two consecutive events.